



# Ultra Low Cost, $\pm 2.0$ g Dual Axis Accelerometer With I<sup>2</sup>C Interface

## MXC6202xJ/K

### FEATURES

- Small low profile package:  
5.5mm x 5.5mm x 1.4mm
- Designed for very low cost applications
- RoHS compliant
- I<sup>2</sup>C Slave, FAST ( $\leq 400$  KHz.) mode
- Power up/down function through I<sup>2</sup>C
- On-chip temperature sensor available
- Eight customer defined 7-bit addresses
- $>50,000$  g shock survival rating
- Most reliable industry proven product due to no moving part in sensor structure

### APPLICATIONS

The MXC6202xJ/K is optimized for motion-sensing and tilt-sensing applications such as gesture recognition, menu and screen navigation and HDD protection for consumer devices including:

**Information Appliances:** – Cell Phones, PDA's, MP3's

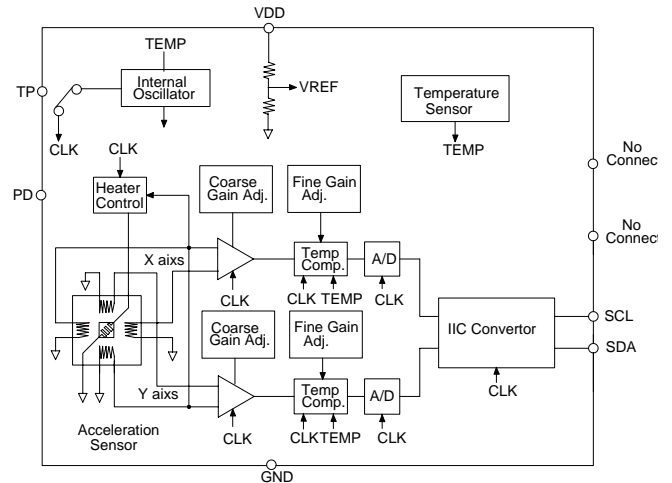
**Consumer Products:** –Pedometers, Blood Pressure Monitor, Digital Cameras

**Gaming Products:**– Joysticks, RF Interfaces, Handheld games, Menu Selection, Tilt Sensing

**GPS:** – Electronic Compass Tilt Correction

### GENERAL DESCRIPTION

The MXC6202xJ/K is an ultra low cost; dual axis accelerometer fabricated on a standard, submicron CMOS process. It is a complete sensing system with on-chip mixed signal processing and integrated I<sup>2</sup>C (Inter IC) bus, allowing the device to be connected directly to a microprocessor eliminating the need for A/D converters or timing resources. It measures acceleration with a full-scale range of  $\pm 2$  g and a sensitivity of 400counts/g @3.0 V at 25°C. It can measure both dynamic acceleration (e.g. vibration)



MXC6202xJ/K FUNCTIONAL BLOCK DIAGRAM

and static acceleration (e.g. gravity). Its design is based on heat convection and requires no solid proof mass.

This design eliminates the stiction problems associated with legacy technologies and provides shock survival greater than 50,000g's. MEMSIC's solid state design leads to significantly lower failure rates in customer applications as well as lower loss due to handling during manufacturing and assembly processes.

It is packaged in a small low profile LCC surface mount package (5.5 mm x 5.5 mm x 1.40 mm with a maximum height of 1.50 mm) and is available for operating temperature ranges of -10°C to +70°C (J) and -40°C to +85°C (K).

The maximum noise floor is  $2.0 \text{ mg}/\sqrt{\text{Hz}}$  allowing signals below 2milli-g to be resolved at 1 Hz bandwidth.

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**ELECTRICAL CHARACTERISTICS** (Measurements @ 25°C, Acceleration = 0 g unless otherwise noted; V<sub>DD</sub> = 3.0V unless otherwise specified)

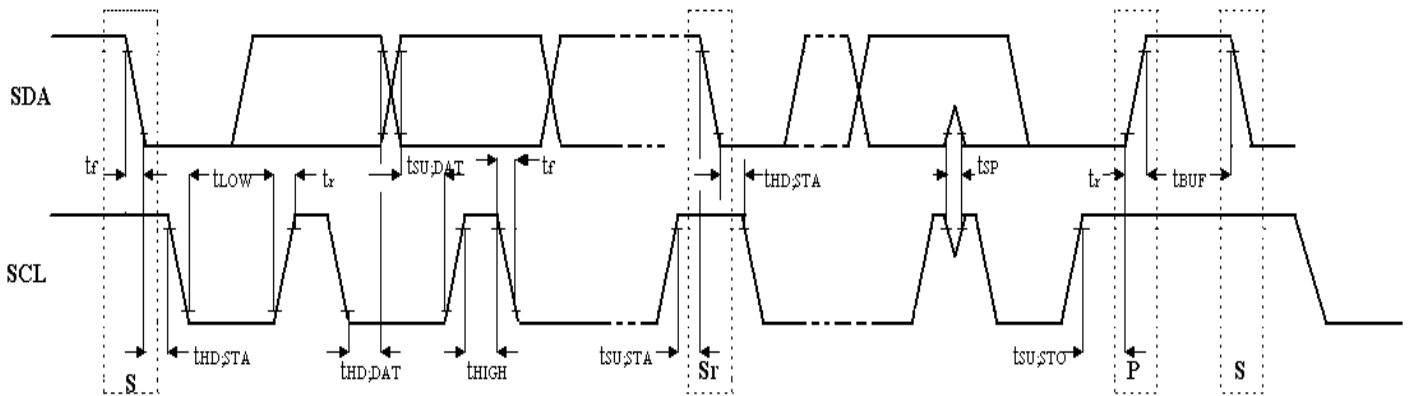
Parameter	Conditions	Min	Typ	Max	Units
Measurement Range <sup>1</sup> (Each Axis)		±2.0			g
Nonlinearity	Best fit straight line		1.0	2.0	% of FS
Alignment Error <sup>2</sup>			±1.0		degrees
Transverse Sensitivity <sup>3</sup>			±2.0		%
Sensitivity		-10		+10	%
		360	400	440	counts/g
Sensitivity Change Over Temperature (Δ from 25°C)	J	-10		+8	%
	K	-20		+8	%
Zero g Offset Bias Level		-0.15	0	0.15	g
		1988	2048	2108	counts
Zero g Offset TC	Δ from 25°C		3.0		mg/°C
Temperature Output		3195	3375	3555	counts
Temperature Output Sensitivity		4.1	4.6	5.1	counts/°C
Noise Density, RMS	within 30Hz		1.0	2.0	mg/√Hz
Resolution	@ 1Hz. BW		1.0		mg
Frequency Response	@ -3dB	25	30	35	Hz
Output Drive Capability	@ 2.7 V – 3.6 V			100	uA
Output Headroom	Output High	2.8			V
	Output Low			0.2	V
Turn-On Time <sup>4</sup>			50	75	mS
Operating Voltage Range		2.7	3.0	3.6	V
Supply Current			2.3		mA
Power Down Current				1.0	uA
Operating Temperature Range	J	-10		+70	°C
	K	-40		+85	°C

**NOTES:**

- <sup>1</sup> Guaranteed by measurement of initial offset and sensitivity
- <sup>2</sup> Alignment error is specified as the angle between the true and indicated axis of sensitivity
- <sup>3</sup> Cross axis sensitivity is the algebraic sum of the alignment and the inherent sensitivity errors
- <sup>4</sup> Output settled to within ± 17mg

## I<sup>2</sup>C INTERFACE I/O CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic Input Low Level	$V_{IL}$		-0.5		0.6	V
Logic Input High Level	$V_{IH}$		1.4			V
Hysteresis of Schmitt Input	$V_{hys}$		0.2			V
Logic Output Low Level	$V_{OL}$				0.4	
Input Leakage Current	$I_i$	$0.1V_{DD} < V_{in} < 0.9V_{DD}$	-10		10	$\mu A$
SCL Clock Frequency	$f_{SCL}$		0		400	kHz
START Hold Time	$t_{HD,STA}$		0.6			$\mu S$
START Setup Time	$t_{SU,STA}$		0.6			$\mu S$
LOW Period of SCL	$t_{LOW}$		1.3			$\mu S$
HIGH Period of SCL	$t_{HIGH}$		0.6			$\mu S$
Data Hold Time	$t_{HD,DAT}$		0		0.9	$\mu S$
Data Setup Time	$t_{SU,DAT}$		0.1			$\mu S$
Rise Time	$t_r$	From $V_{IL}$ to $V_{IH}$			0.3	$\mu S$
Fall Time	$t_f$	From $V_{IH}$ to $V_{IL}$			0.3	$\mu S$
Bus Free Time Between STOP and START	$t_{BUF}$		1.3			$\mu S$
STOP Setup Time	$t_{SU,STO}$		0.6			$\mu S$

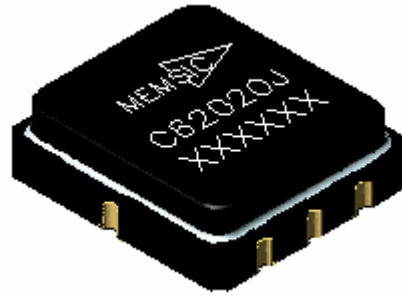


Timing Definition

**ABSOLUTE MAXIMUM RATINGS\***

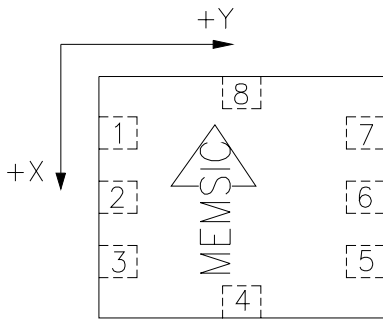
Supply Voltage (V<sub>DD</sub>).....-0.5 V to +7.0V  
 Storage Temperature.....-65°C to +150°C  
 Acceleration.....50,000 g

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



**Pin Description: LCC-8 Package**

Pin	Name	Description	I/O
1	NC	Do Not Connect	NC
2	COM	Connected to Ground	I
3	GND	Connected to Ground	I
4	TEST	Do Not Connect	NC
5	VDD2	Power Supply for I <sup>2</sup> C bus	I
6	SCL	Serial Clock Line for I <sup>2</sup> C bus	I
7	SDA	Serial Data Line for I <sup>2</sup> C bus	I/O
8	V <sub>DD</sub>	2.7 V to 3.6 V	I



Top View  
(Not to Scale)

**Note:** The MEMSIC logo's arrow indicates the -X sensing direction of the device. The +Y sensing direction is rotated 90° away from the +X direction following the right-hand rule.

**Ordering Guide:**

**MXC6202xJV**

Package type:

Code	Type
V	LCC8 RoHS compliant

Performance Grade:

Code	Temp	Output Range
J	-10~70°C	I <sup>2</sup> C:4096counts
K	-40~85°C	I <sup>2</sup> C:4096counts

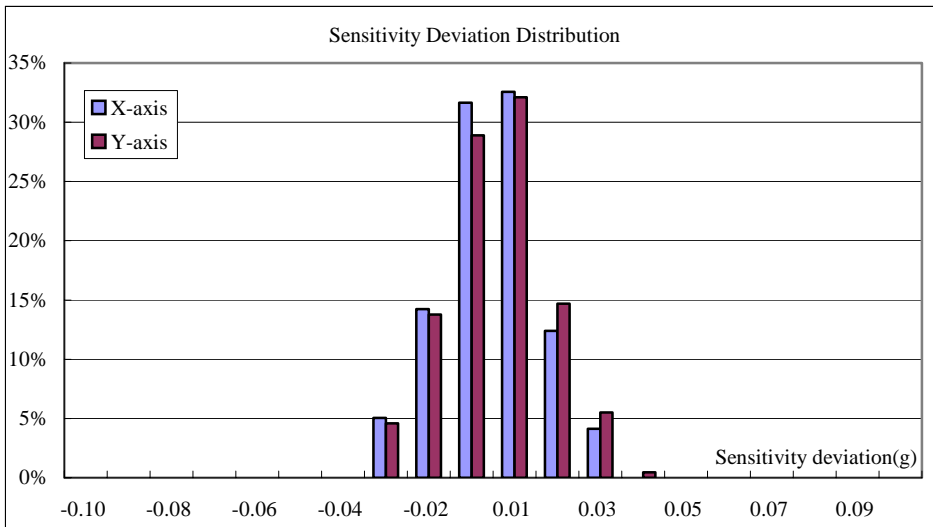
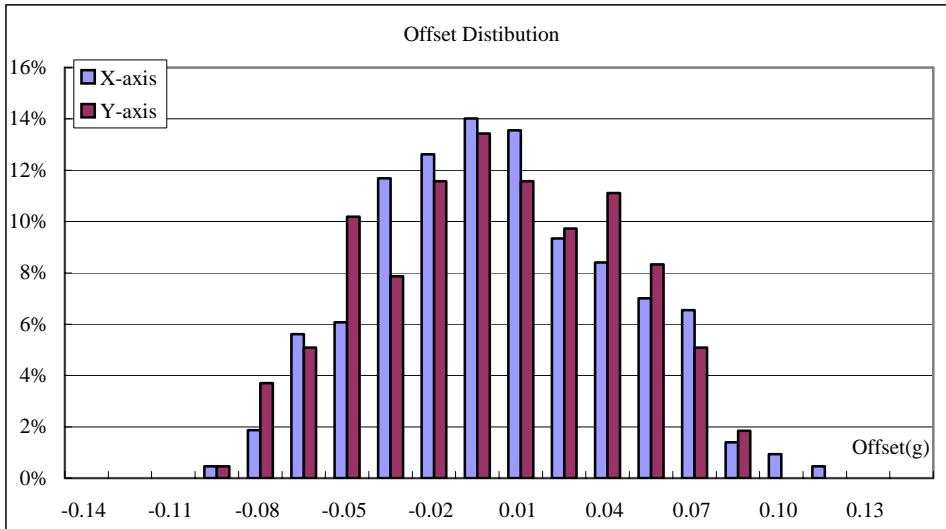
Address code: 0 to 7

Number	Address
0	20H
1	22H
2	24H
3	26H
4	28H
5	2AH
6	2CH
7	2EH

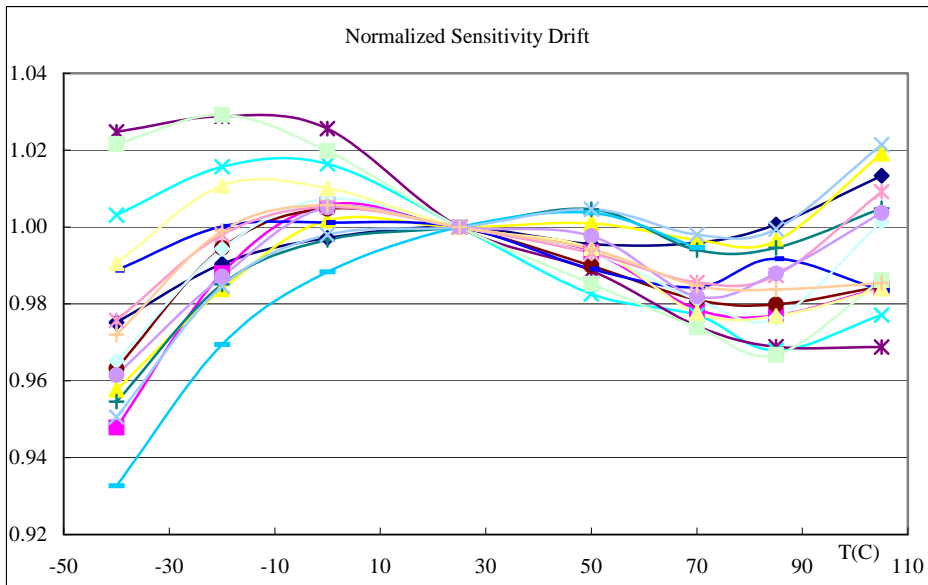
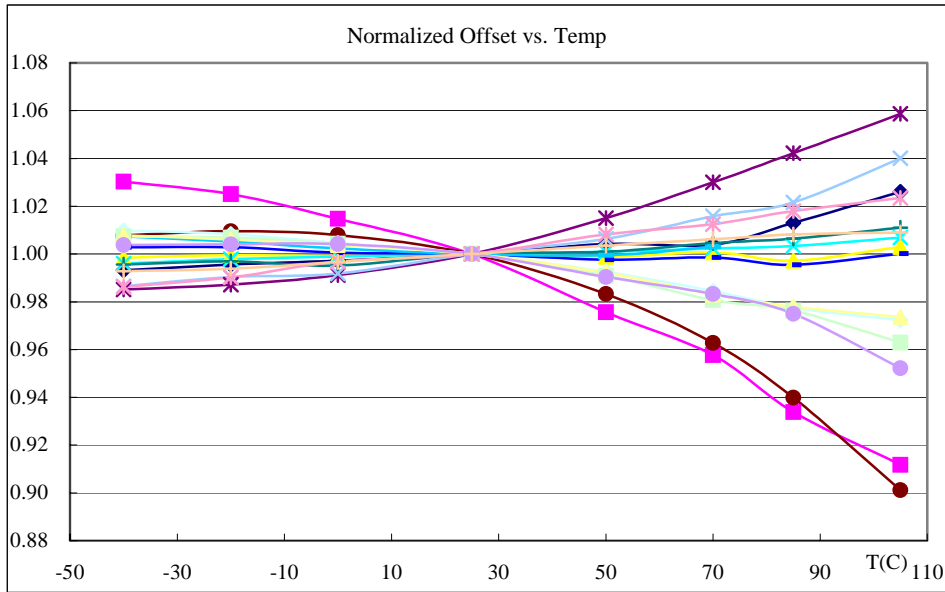
All parts are shipped in tape and reel packaging.

**Caution:** ESD (electrostatic discharge) sensitive device.

**TYPICAL CHARACTERISTICS, % OF UNITS (@ 25°C, V<sub>DD</sub> = 3V)**



# OVER TEMPERATURE CHARACTERISTICS



## THEORY OF OPERATION

The MEMSIC device is a complete dual-axis acceleration measurement system fabricated on a monolithic CMOS IC process. The device operation is based on heat transfer by natural convection and operates like other accelerometers except that the proof mass in the MEMSIC sensor is a gas.

A single heat source, centered in the silicon chip is suspended across a cavity. Equally spaced aluminum/polysilicon thermopiles (groups of thermocouples) are located equidistantly on all four sides of the heat source (dual axis). Under zero acceleration, a temperature gradient is symmetrical about the heat source, so that the temperature is the same at all four thermopiles, causing them to output the same voltage.

Acceleration in any direction will disturb the temperature profile, due to free convection heat transfer, causing it to be asymmetrical. The temperature, and hence voltage output of the four thermopiles will then be different. The differential voltage at the thermopile outputs is directly proportional to the acceleration. There are two identical acceleration signal paths on the accelerometer, one to measure acceleration in the x-axis and one to measure acceleration in the y-axis. Please visit the MEMSIC website at [www.memsic.com](http://www.memsic.com) for a picture/graphic description of the free convection heat transfer principle.

## MXC6202xJ/K PIN DESCRIPTIONS

**V<sub>DD</sub>** – This is the supply input for the circuits and the sensor heater in the accelerometer. The DC voltage should be between 2.7 and 3.6 volts. Refer to the section on PCB layout and fabrication suggestions for guidance on external parts and connections recommended.

**GND**– This is the ground pin for the accelerometer.

**COM**– This pin should be connected to ground.

**TEST**– Do Not Connect, factory use only.

**V<sub>DD2</sub>**– This pin is the I<sup>2</sup>C input digital power supply, the voltage on this pin determines the I<sup>2</sup>C bus logic voltage, and is 1.8V compatible. Note: The voltage on this pin should be equal to or less than the voltage on V<sub>DD</sub>. Power should be applied to V<sub>DD</sub> first unless V<sub>DD2</sub> power supply voltage equals V<sub>DD</sub>, in which case power may be applied to V<sub>DD</sub> and V<sub>DD2</sub> simultaneously.

**SDA**– This pin is the I<sup>2</sup>C serial data line, and operates in FAST (400 KHz.) mode.

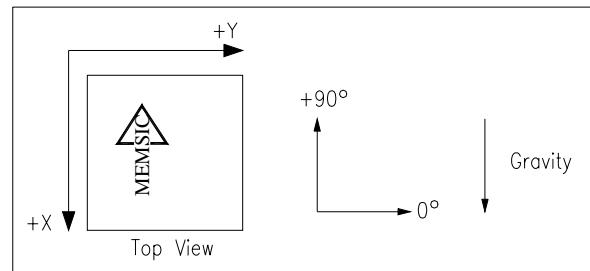
**SCL**– This pin is the I<sup>2</sup>C serial clock line, and operates in FAST (400 KHz.) mode.

## DISCUSSION OF TILT APPLICATIONS AND RESOLUTION

**Tilt Applications:** One of the most popular applications for the MEMSIC accelerometer product line is in tilt/inclination measurement. An accelerometer uses the force of gravity as an input to determine the inclination angle of an object.

A MEMSIC accelerometer is most sensitive to changes in position, or tilt, when the accelerometer's sensitive axis is perpendicular to the force of gravity, or parallel to the Earth's surface. Similarly, when the accelerometer's axis is parallel to the force of gravity (perpendicular to the Earth's surface), it is least sensitive to changes in tilt.

The following table and figure help to illustrate the output changes in the X- and Y-axes as the unit is tilted from +90° to 0°. Notice that when one axis has a small change in output per degree of tilt (in mg), the second axis has a large change in output per degree of tilt. The complementary nature of these two signals permits low cost accurate tilt sensing to be achieved with the MEMSIC device (reference application note AN-00MX-007).



*Accelerometer Position Relative to Gravity*

X-Axis Orientation To Earth's Surface (deg.)	X-Axis		Y-Axis	
	X Output (g)	Change per deg. of tilt (mg)	Y Output (g)	Change per deg. of tilt (mg)
90	1.000	0.15	0.000	17.45
85	0.996	1.37	0.087	17.37
80	0.985	2.88	0.174	17.16
70	0.940	5.86	0.342	16.35
60	0.866	8.59	0.500	15.04
45	0.707	12.23	0.707	12.23
30	0.500	15.04	0.866	8.59
20	0.342	16.35	0.940	5.86
10	0.174	17.16	0.985	2.88
5	0.087	17.37	0.996	1.37
0	0.000	17.45	1.000	0.15

*Changes in Tilt for X- and Y-Axes*

## RESOLUTION

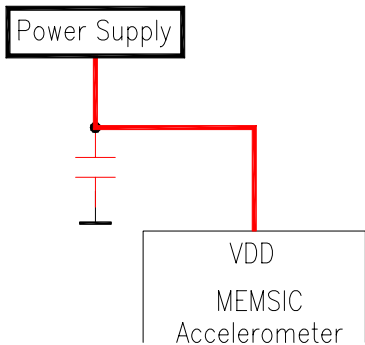
The accelerometer resolution is limited by noise. The output noise will vary with the measurement bandwidth. With the reduction of the bandwidth, by applying an external low pass filter, the output noise drops. Reduction of bandwidth will improve the signal to noise ratio and the resolution. The output noise scales directly with the square root of the measurement bandwidth. The maximum amplitude of the noise, its peak-to-peak value, approximately defines the worst case resolution of the measurement. With a simple RC low pass filter, the rms noise is calculated as follows:

$$\text{Noise}(mg \text{ rms}) = \text{Noise}(mg / \sqrt{\text{Hz}}) * \sqrt{(\text{Bandwidth}(\text{Hz}) * 1.6)}$$

The peak-to-peak noise is approximately equal to 6.6 times the rms value (for an average uncertainty of 0.1%).

## HARDWARE DESIGN CONSIDERATIONS

1. One capacitor is recommended for best rejection of power supply noise (reference figure below). The capacitor should be located as close as possible to the device supply pin (V<sub>DD</sub>). The capacitor lead length should be as short as possible, and a surface mount capacitor is preferred. For typical applications, the capacitor can be ceramic 0.1 µF.



Power supply noise rejection

2. Robust low inductance ground wiring should be used.
3. Care should be taken to ensure there is “thermal symmetry” on the PCB immediately surrounding the MEMSIC device and that there is no significant heat source nearby. Based on the experiment, with a 85° C heating source at 15mm away of MEMSIC device, the offset change will be within 0.7g.
4. A metal ground plane should be added directly beneath the MEMSIC device. The size of the

plane should be similar to the MEMSIC device’s footprint and be as thick as possible.

5. Vias can be added symmetrically around the ground plane. These vias will increase the thermal isolation of the device from the rest of the PCB and improve performance.

## SOFTWARE DESIGN CONSIDERATION

We recommended that the following software limiter filter be used in the acceleration signal process routine in order to further reduce the noise on the I2C bus:

```

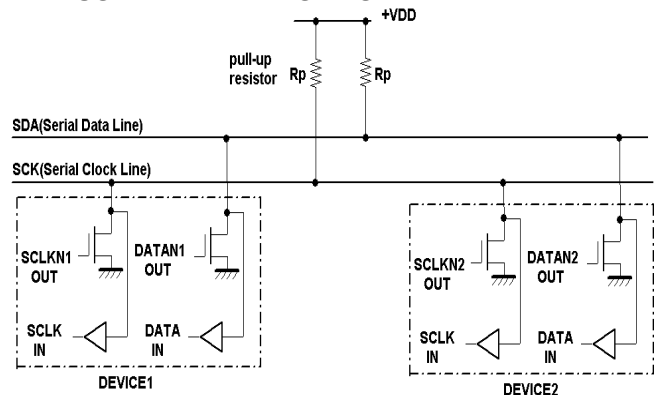
Int iAccReal[0x02]; //Real-time acceleration data array
Int iAccFilter; //Filtered acceleration data
SoftwareLimiterFilter()
{
if (abs(iAccReal[0x00]-iAccReal[0x01])<0x80) then
iAccFilter=iAccReal[0x00];
iAccReal[0x01]= iAccReal[0x00];
}
    
```

## I<sup>2</sup>C INTERFACE DESCRIPTION

A slave mode I<sup>2</sup>C (or Inter IC bus) circuit has been implemented into the MEMSIC thermal accelerometer as a standard interface for customer applications. The A/D converter and MCU functionality have been added to the MEMSIC sensor, thereby increasing ease-of-use, and lowering power consumption, footprint and total solution cost.

The I<sup>2</sup>C is an industry standard bi-directional two-wire interface bus. A master I<sup>2</sup>C device can operate READ/WRITE controls to an unlimited number of devices on the bus by proper addressing. The MEMSIC accelerometer operates only in a slave mode, i.e. only responding to calls by a master device

## I<sup>2</sup>C BUS CHARACTERISTICS



I<sup>2</sup>C Bus

The two wires in I<sup>2</sup>C bus are called SDA (serial data line) and SCL (serial clock line). In order for a data transfer to start, the bus has to be free, which is defined by both wires in a HIGH output state. Due to the open-drain/pull-up resistor structure and wired

Boolean “AND” operation, any device on the bus can pull lines low and overwrite a HIGH signal. The data on the SDA line has to be stable during the HIGH period of the SCL line. In other words, valid data can only change when the SCL line is LOW.

**I<sup>2</sup>C BUS DATA TRANSFER**

A data transfer is started with a “START” condition and ended with a “STOP” condition. A “START” condition is defined by a HIGH to LOW transition on the SDA line while SCL line is HIGH. A “STOP” condition is defined by a LOW to HIGH transition on the SDA line while SCL line is HIGH. All data transfer in I<sup>2</sup>C system is 8-bits long. Each byte has to be followed by an acknowledge bit. Each data transfer involves a total of 9 clock cycles. Data is transferred starting with the most significant bit (MSB). After a “START” condition, the master device calls a specific slave device, in our case, the MEMSIC accelerometer with a 7-bit device address. To avoid potential address conflict, either by ICs from other manufacturers or by other MEMSIC accelerometers on the same bus, a total of 8 different addresses can be programmed into a MEMSIC device at the factory. Following the 7-bit address, the 8<sup>th</sup> bit determines the direction of data transfer: [1] for READ and [0] for WRITE. After being addressed, the available MEMSIC device being called will respond by an “Acknowledge” signal, which is pulling SDA line LOW.

In order to read an acceleration signal, the master device should operate a WRITE action with a code of “[xxxxxx0]” into the MEMSIC device 8-bit internal register.

Bit	Name	Function
0	PD (Power Down)	Power down [1]/on [0]
1	Reserved	NC
2	BGTST (bandgap test)	Bandgap test [1]/normal[0]
3	TOEN (temperature out enable)	Temp Out EN [1]/disable[0]

BGTST is used to calibrate the temperature output signal's initial offset. By flipping the BGTST bit and taking the average of two readings, the temperature output initial offset will be calibrated to within datasheet specifications.

After writing code of “[xxxxxx0]” into the control register, if a “READ” signal is received, during next 9 clock cycles, the MEMSIC device being called will transfer 8-bits of data to the I<sup>2</sup>C bus. If an “Acknowledge” by master device is received, the MEMSIC device will continue to transfer the next byte. The same procedure repeats until 5 bytes of data are transferred to master device. Those 5 bytes of data are defined as following (“T” is temperature output):

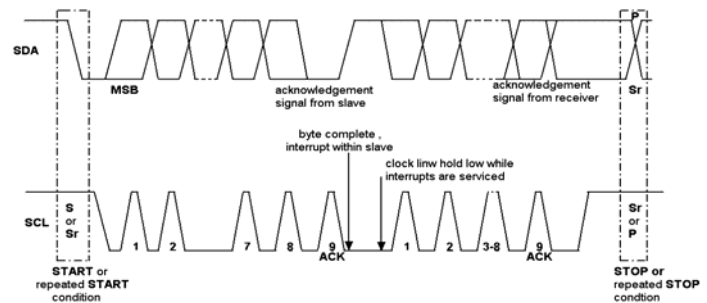
1. Internal register
2. MSB X/T axis

3. LSB X/T axis
4. MSB Y axis
5. LSB Y axis

Even though each axis consists of two bytes, which are 16-bits of data, the actual accelerometer resolution is limited to 12bits. Unused MSB's will be simply filled by “0”s.

Note that the temperature output shares the same registers with the X channel output. The implementer can select which signal needs to be read out by using the TOEN bit.

The master can stop slave data transfer after any of the five bytes by not sending an acknowledge command and followed by a “STOP” condition.



*Data transfer*

**POWER DOWN MODE**

The MEMSIC accelerometer can enter a power down mode by the master device writing a code of “[xxxxxx1]” into the accelerometer’s internal register. A wake up operation is performed when the master writes into the same register a code of “[xxxxxx0]”. Note that it needs about 50mS (typical) for power up time.

**EXAMPLE OF DATA COMMUNICATION**

**First cycle:** START followed by a calling to slave address “[0010xxx]” to WRITE (8<sup>th</sup> SCL, SDA keep low). “[xxx]” Is determined by factory programming, a total of 8 different addresses are available.

**Second cycle:** After an acknowledge signal is received by the master device (MEMSIC device pulls SDA line low during 9<sup>th</sup> SCL pulse), the master device sends “[00000000]” as the target address to be written into. The MEMSIC device should acknowledge at the end (9<sup>th</sup> SCL pulse). Note: since the MEMSIC device has only one internal register that can be written into, user should always indicate “[00000000]” as the write address.

**Third cycle:** Master device writes to internal MEMSIC device memory code “[xxxxxx0]” as a wake-up call. The MEMSIC device should send an acknowledge

signal. A STOP command indicates the end of write operation. A 100mS (typical) wait period should be given to the MEMSIC device to return from a power-down mode. The delay value depends on the type of MEMSIC device. Generally speaking, low power products tend to have longer startup time.

**Fourth cycle:** The master device sends a START command followed by calling MEMSIC device address with a WRITE (8<sup>th</sup> SCL, SDA keep low). An “acknowledge” should be sent by the MEMSIC device at the end.

**Fifth cycle:** The master device writes to the MEMSIC device a “[00000000]” as the starting address for which internal memory is to be read. Since “[00000000]” is the address of internal control register, reading from this address can serve as a verification of operation and to confirm the write command has been successful. Note: the starting address in principle can be any of the 5 addresses. For example, user can start read from address “[0000001]”, which is X channel MSB.

**Sixth cycle:** The master device calls the MEMSIC device address with a READ (8<sup>th</sup> SCL cycle SDA line high). The MEMSIC device should acknowledge at the end.

**Seventh cycle:** The master device cycles the SCL line, first addressed memory data appears on SDA )

line. If in step 7, “[00000000]” was sent, internal control register data should appear (in the following steps, this case is assumed). The master device should send an acknowledgement at the end.

**Eighth cycle:** The master device continues to cycle the SCL line, the next byte of internal memory should appear on the SDA line (MSB of X channel). The internal memory address pointer automatically moves to the next byte. The master acknowledges.

**Ninth cycle:** LSB of X channel. In the case that the TOEN bit of internal register was set to “1”, the MSB and LSB of TOUT (temperature) should appear in the last two steps.

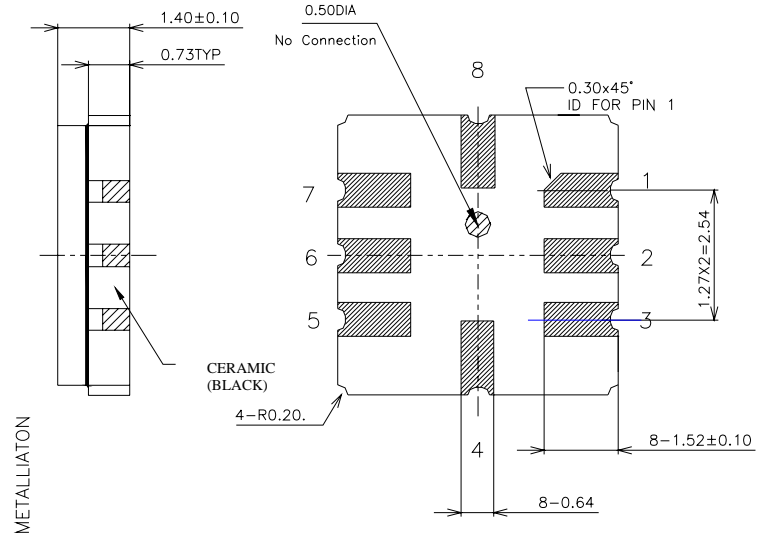
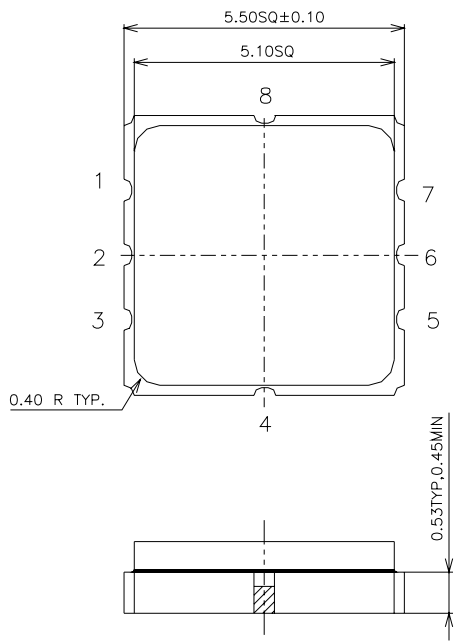
**Tenth cycle:** MSB of Y channel.

**Eleventh cycle:** LSB of Y channel.

The master ends communications by sending a NO acknowledge and followed by a STOP command. Note: if the master device continues to cycle the SCL line, the memory pointer will go to sixth and seventh positions, which always have “[00000000]”. After seventh position, pointer will go to zero again.

**Optional:** The master powers down the MEMSIC device by writing into the internal control register. (See step 1 through 4 for WRITE operation)

# PACKAGE DRAWING



- NOTES :
1. UNIT:mm
  2. TOLERANCE UNLESS OTHERWISE SPECIFIED WITHIN +/-0.20

Package Outline