DATA SHEET

PCA9535

16-bit I^{2}C and SMBus, low power I/O port with interrupt

Product data sheet
Supersedes data of 2003 Jun 27

2004 Sep 30

Philips
Semiconductors

16-bit I²C and SMBus, low power I/O port with interrupt PCA9535

FEATURES

- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity inversion register
- Active LOW interrupt output
- Low stand-by current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 16 I/O pins which default to 16 inputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Offered in three different packages: SO24, TSSOP24, and HVQFN24

DESCRIPTION

The PCA9535 is a 24-pin CMOS device that provide 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C/SMBus applications and was developed to enhance the Philips family of I²C I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, LEDs, fans, etc.

The PCA9535 consist of two 8-bit Configuration (Input or Output selection); Input, Output and Polarity inversion (Active HIGH or Active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion Register. All registers can be read by the system master. Although pin-to-pin and I²C address compatible with the PCF8575, software changes are required due to the enhancements and are discussed in Application Note AN469.

The PCA9535 is identical to the PCA9555 except for the removal of the internal I/O pull-up resistor which greatly reduces power consumption when the I/Os are held LOW.

The PCA9535 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I²C address and allow up to eight devices to share the same I²C/SMBus. The fixed I²C address of the PCA9535 is the same as the PCA9554 allowing up to eight of these devices in any combination to share the same I²C/SMBus.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
24-Pin Plastic SO	–40 °C to +85 °C	PCA9535D	PCA9535D	SOT137-1
24-Pin Plastic TSSOP	–40 °C to +85 °C	PCA9535PW	PCA9535PW	SOT355-1
24-Pin Plastic HVQFN	–40 °C to +85 °C	PCA9535BS	9535	SOT616-1

Standard packing quantities and other packing data are available at *www.standardproducts.philips.com/packaging*.

I²C is a trademark of Philips Semiconductors Corporation.
SMBus as specified by the Smart Battery System Implementers Forum is a derivative of the Philips I²C patent.

PIN CONFIGURATION — SO, TSSOP

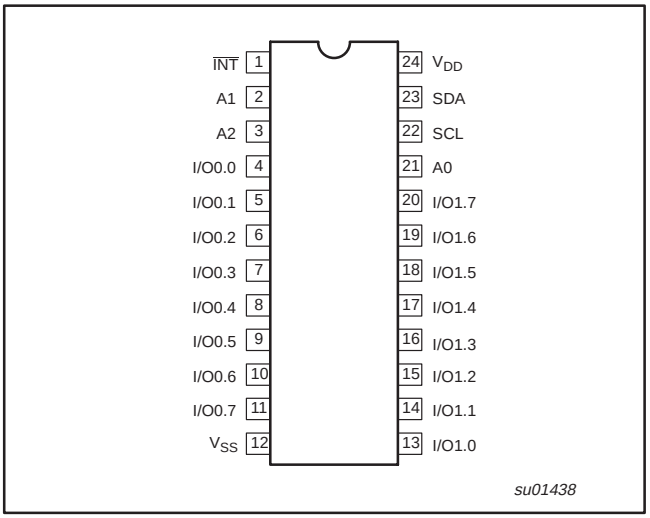


Figure 1. Pin configuration — SO, TSSOP

PIN CONFIGURATION —HVQFN

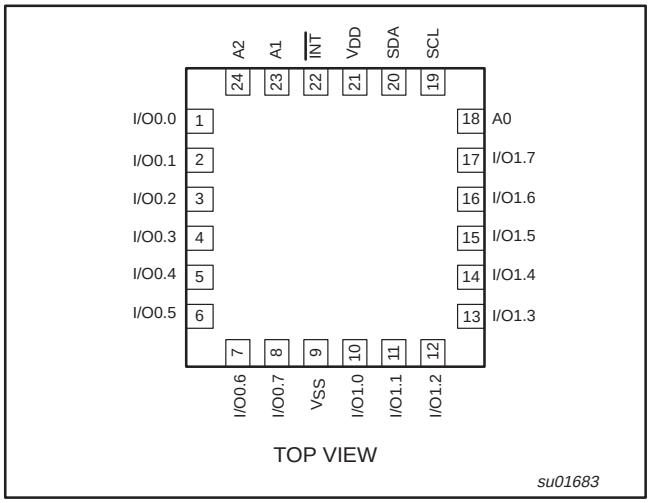


Figure 2. Pin configuration — HVQFN

PIN DESCRIPTION

SO, TSSOP PIN NUMBER	HVQFN PIN NUMBER	SYMBOL	FUNCTION
1	22	$\overline{INT}$	Interrupt output (open drain)
2	23	A1	Address input 1
3	24	A2	Address input 2
4–11	1–8	I/O0.0–I/O0.7	I/O0.0 to I/O0.7
12	9	V_{SS}	Supply ground
13–20	10–17	I/O1.0–I/O1.7	I/O1.0 to I/O1.7
21	18	A0	Address input 0
22	19	SCL	Serial clock line
23	20	SDA	Serial data line
24	21	V_{DD}	Supply voltage

BLOCK DIAGRAM

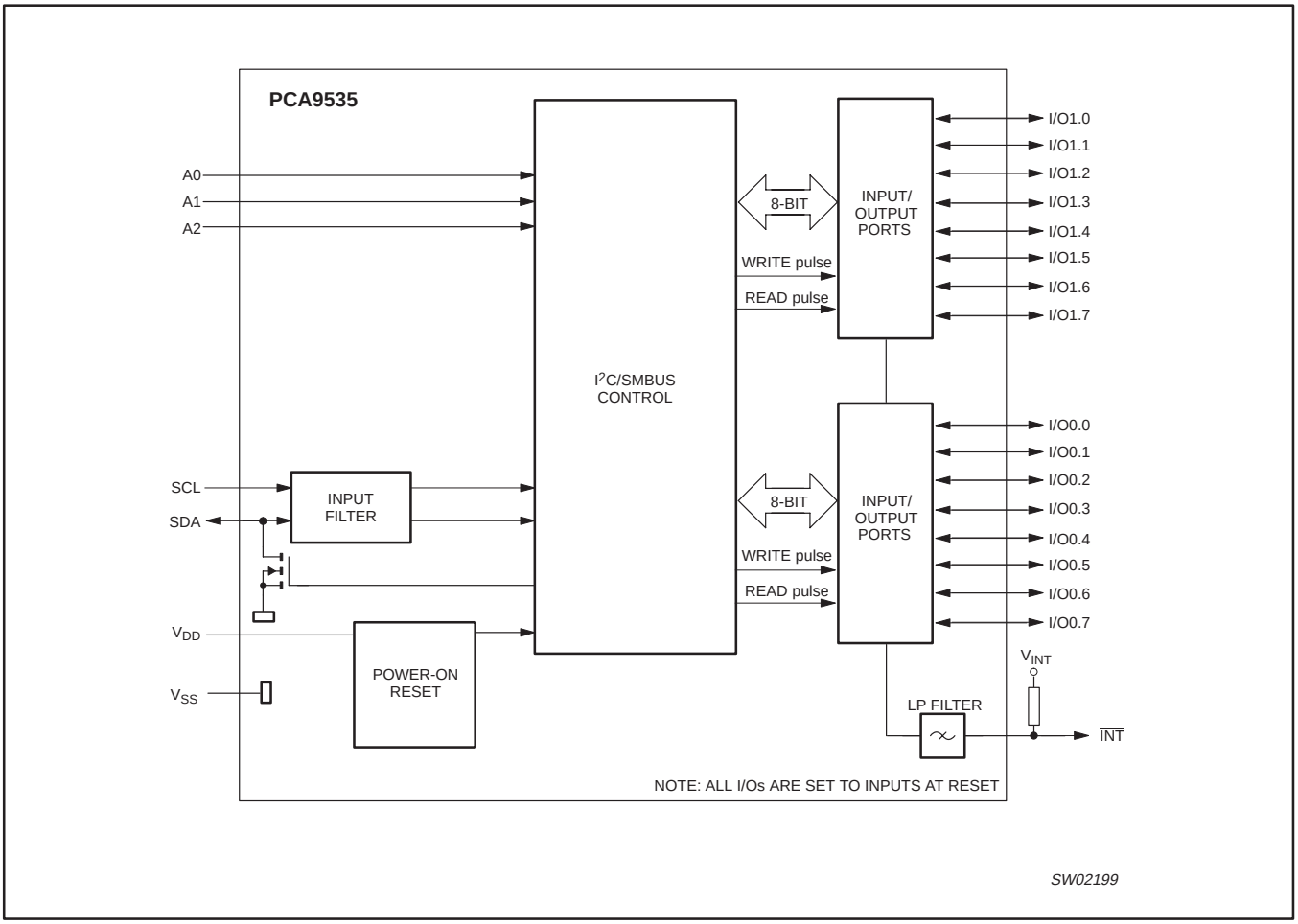
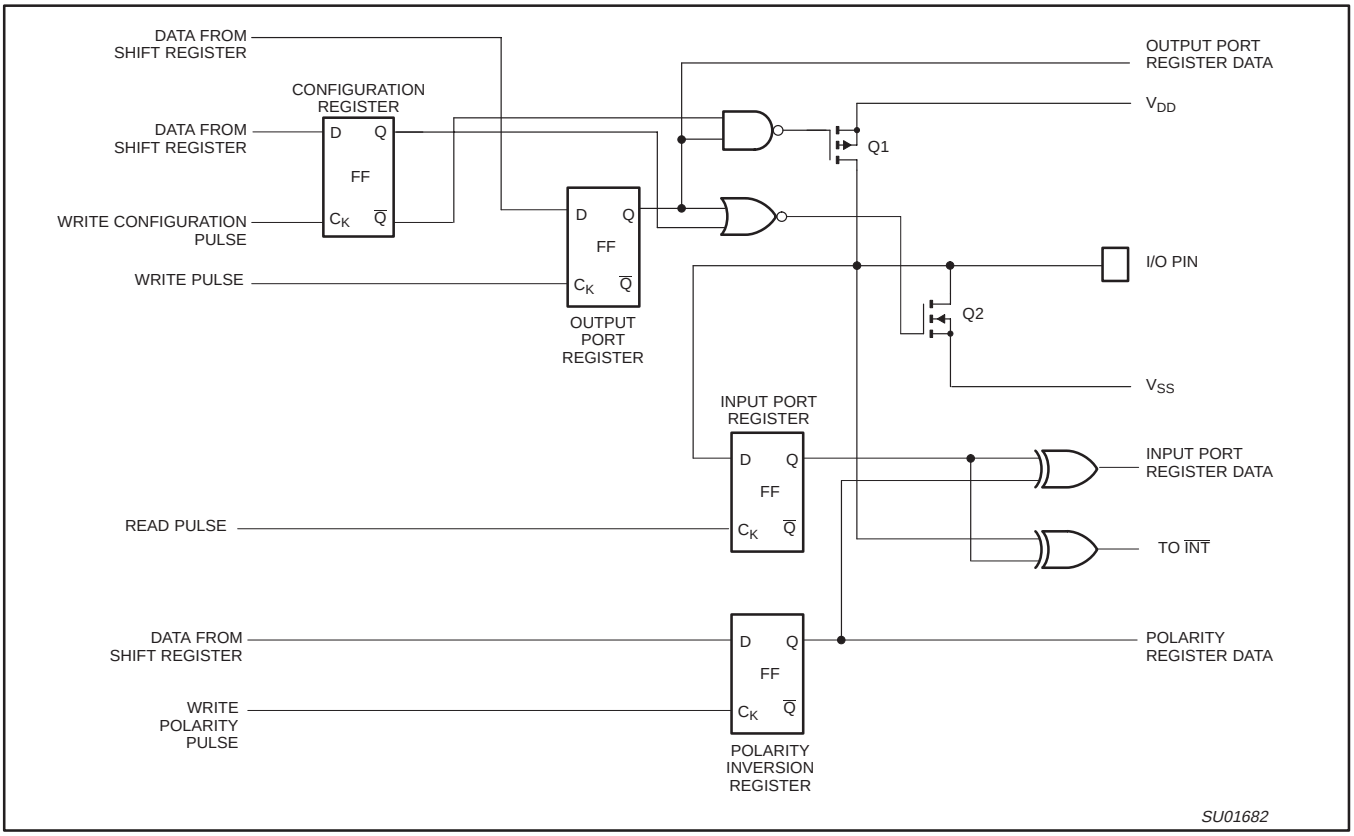


Figure 3. Block diagram

SIMPLIFIED SCHEMATIC OF I/Os



NOTE: At Power-on Reset, all registers return to default values.

Figure 4. Simplified schematic of I/Os

I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low impedance path that exists between the pin and either V_{DD} or V_{SS}.

REGISTERS

Command Byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity inversion port 0
5	Polarity inversion port 1
6	Configuration port 0
7	Configuration port 1

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Registers 0 and 1 — Input Port Registers

bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	IO.0
default	X	X	X	X	X	X	X	X
bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
default	X	X	X	X	X	X	X	X

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value ‘X’ is determined by the externally applied logic level.

Registers 2 and 3 — Output Port Registers

bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
default	1	1	1	1	1	1	1	1
bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
default	1	1	1	1	1	1	1	1

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Register 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Registers 4 and 5 — Polarity Inversion Registers

bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
default	0	0	0	0	0	0	0	0
bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
default	0	0	0	0	0	0	0	0

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with ‘1’), the Input Port data polarity is inverted. If a bit in this register is cleared (written with a ‘0’), the Input Port data polarity is retained.

Registers 6 and 7 — Configuration Registers

bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
default	1	1	1	1	1	1	1	1
bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set (written with ‘1’), the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared (written with ‘0’), the corresponding port pin is enabled as an output. At reset the device’s ports are inputs.

POWER-ON RESET

When power is applied to V_{DD}, an internal power-on reset holds the PCA9535 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9535 registers and SMBus state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operaing voltage.

DEVICE ADDRESS

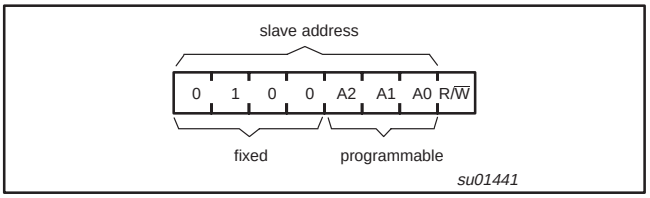


Figure 5. PCA9535 address

BUS TRANSACTIONS

Writing to the port registers

Data is transmitted to the PCA9535 by sending the device address and setting the least significant bit to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the PCA9535 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figures 6 and 7). For example, if the first byte is sent to Output Port (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

Reading the port registers

In order to read data from the PCA9535, the bus master must first send the PCA9535 address with the least significant bit set to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again but this time, the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PCA9535 (see Figures 8 , 9, and 10). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.

Interrupt Output

The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the input port register is read (see Figure 9). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

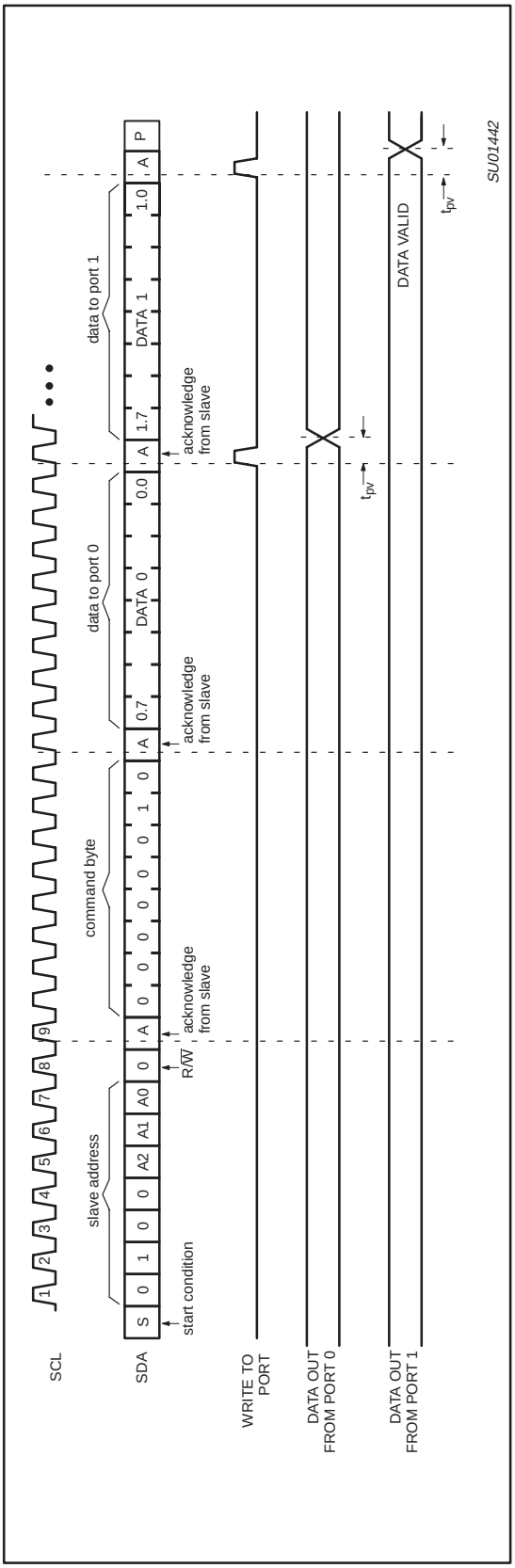


Figure 6. WRITE to output port registers

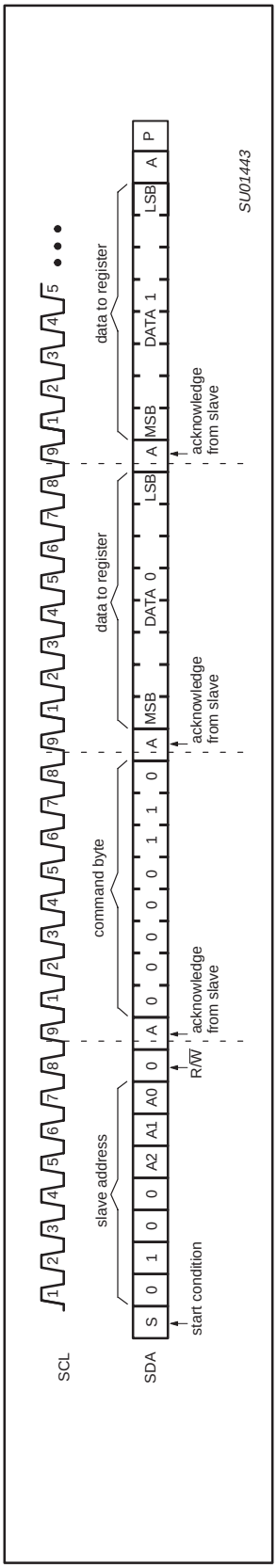
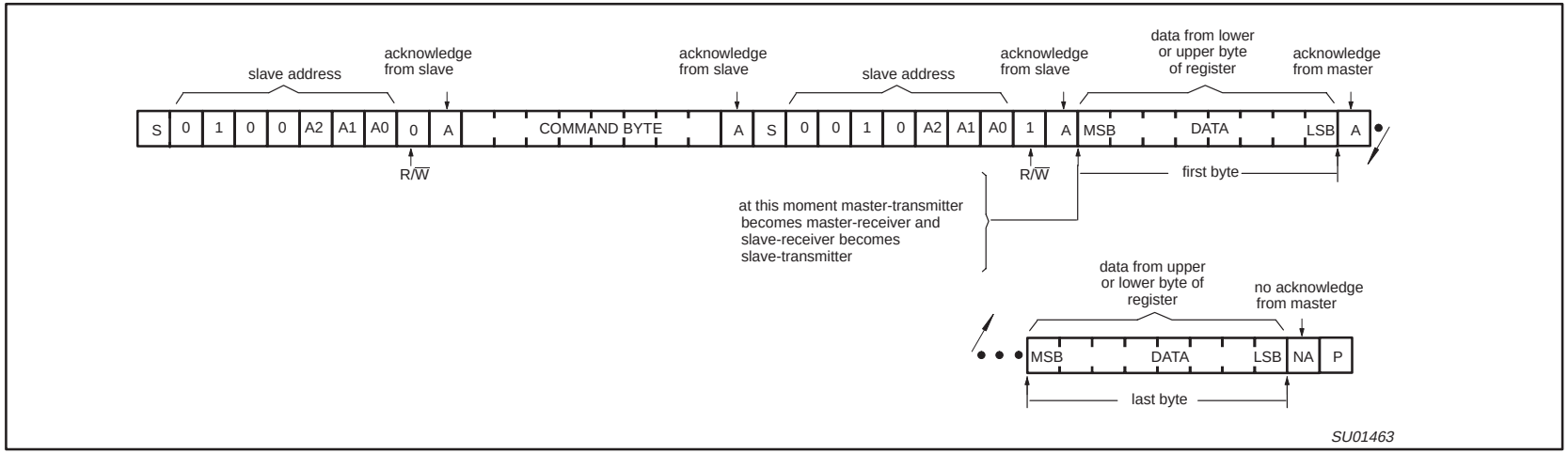
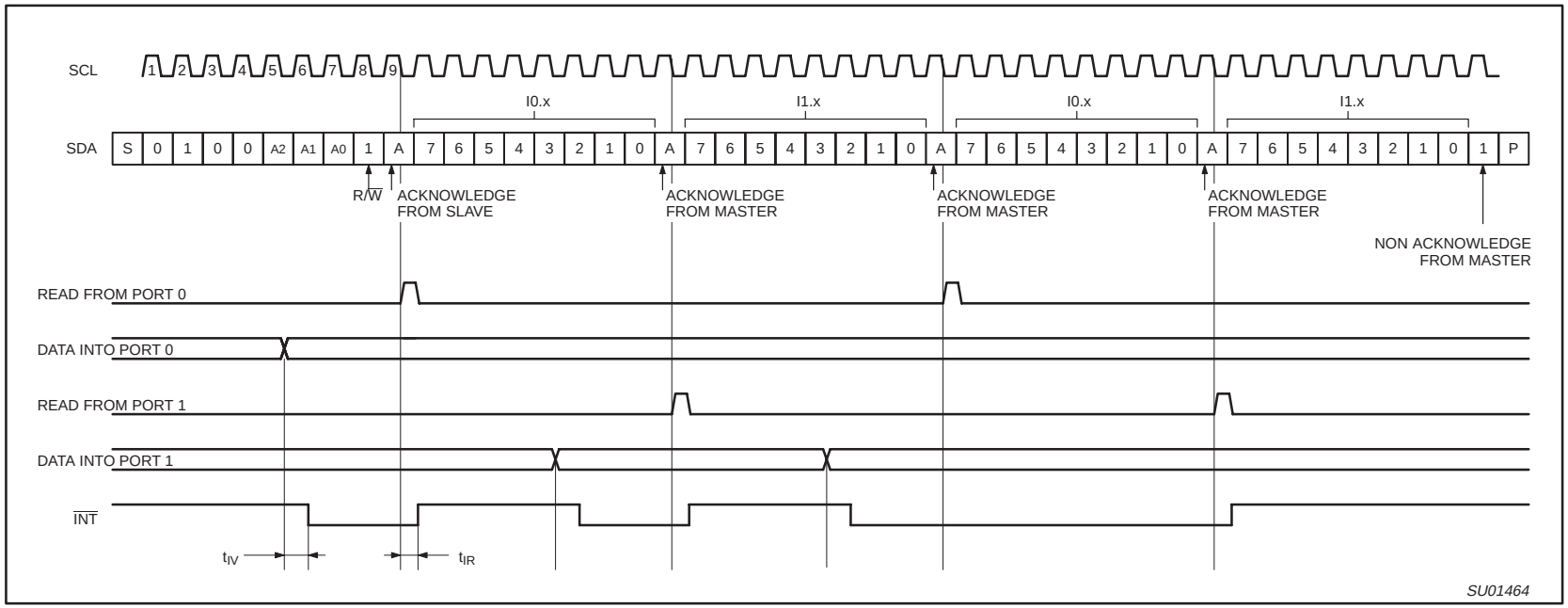


Figure 7. WRITE to configuration registers



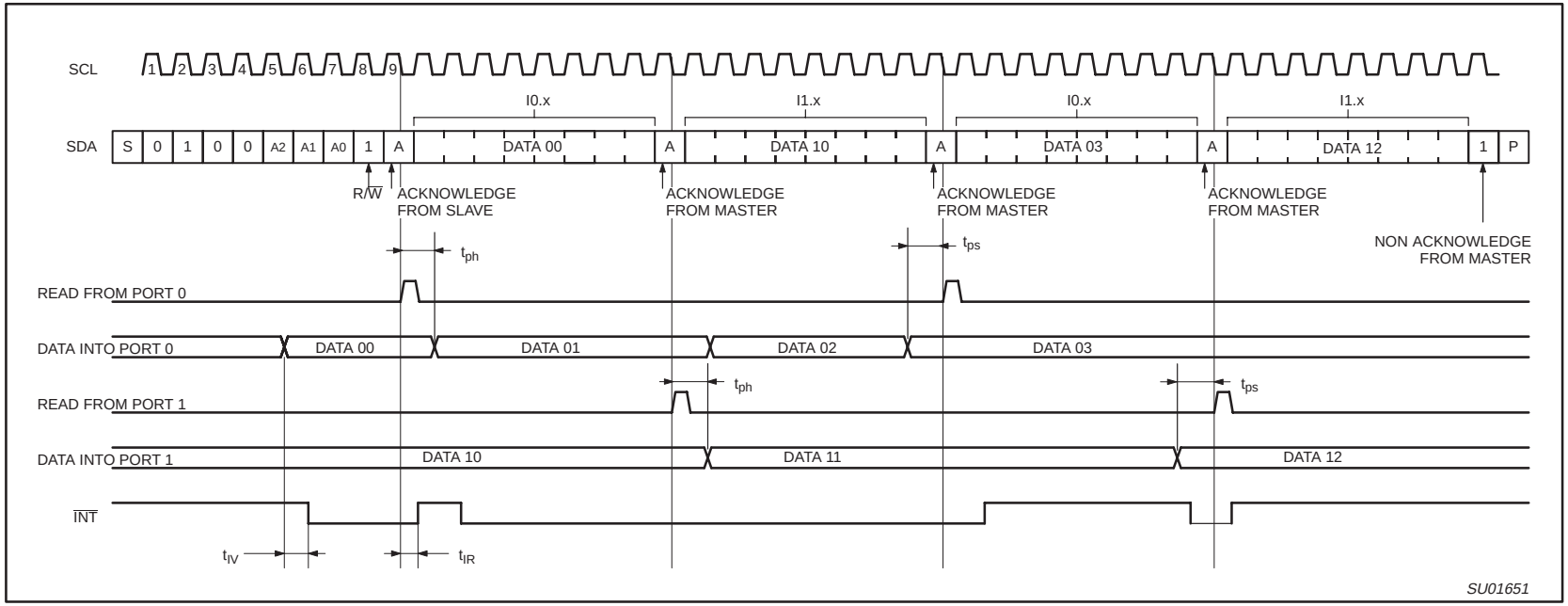
NOTE: Transfer can be stopped at any time by a STOP condition.

Figure 8. READ from register



NOTES: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to 00 (read input port port register).

Figure 9. READ input port register — scenario 1



NOTES: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to 00 (read input port port register).

Figure 10. READ input port register — scenario 2

TYPICAL APPLICATION

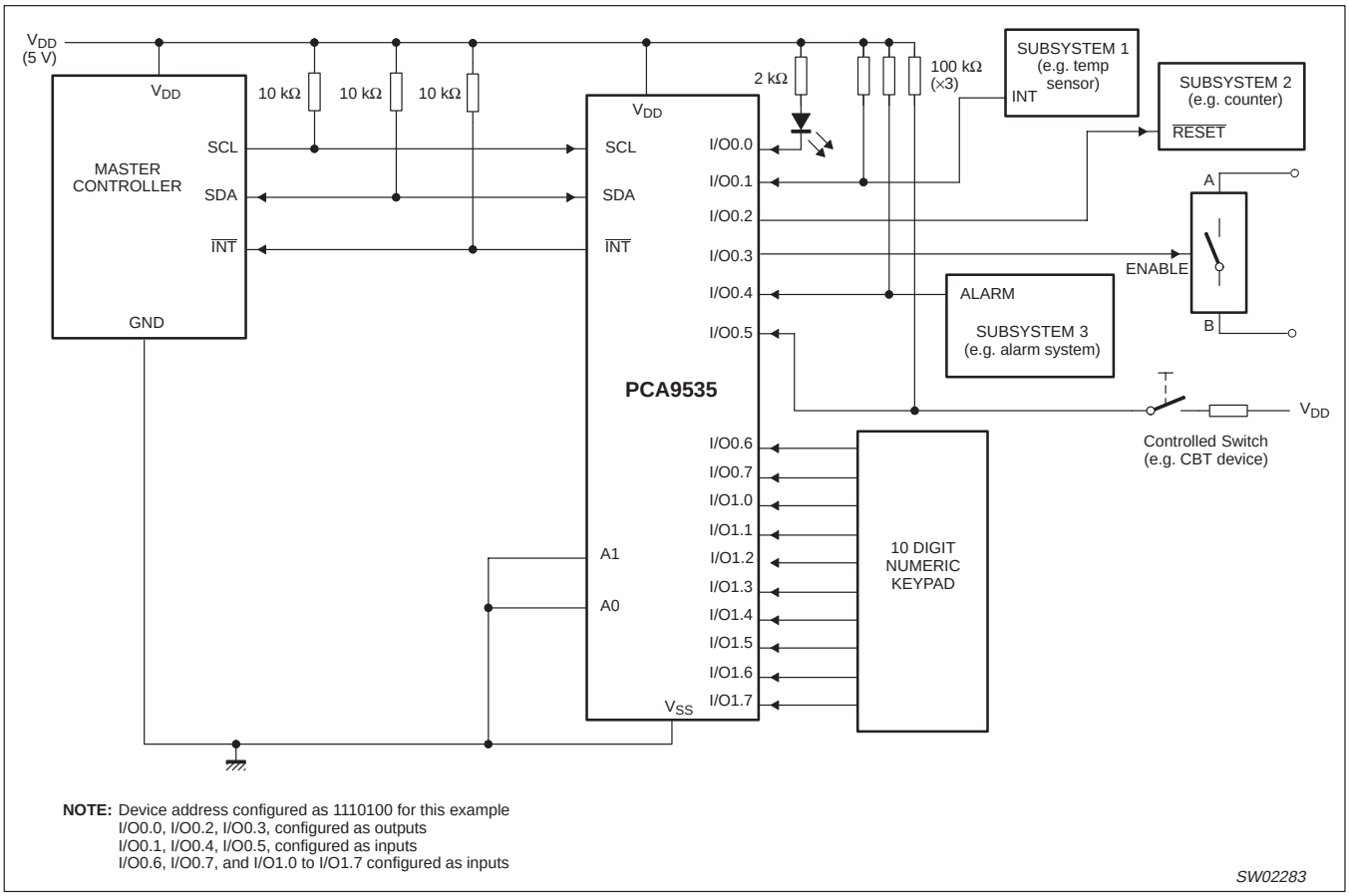


Figure 11. Typical application

Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V_{IN} is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_{IN} becomes lower than V_{DD} and is specified as ΔI_{DD} in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 12 shows a high value resistor in parallel with the LED. Figure 13 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{DD} and prevents additional supply current consumption when the LED is off.

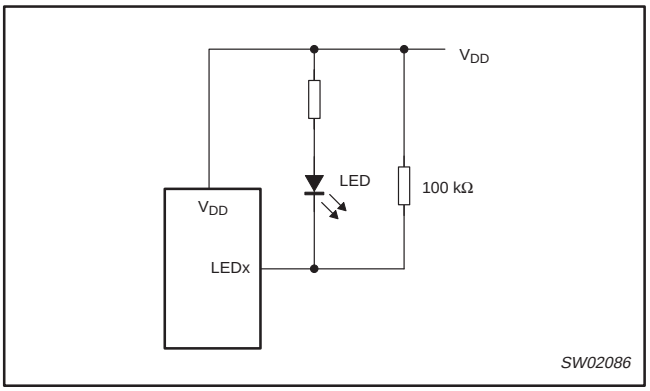


Figure 12. High value resistor in parallel with the LED

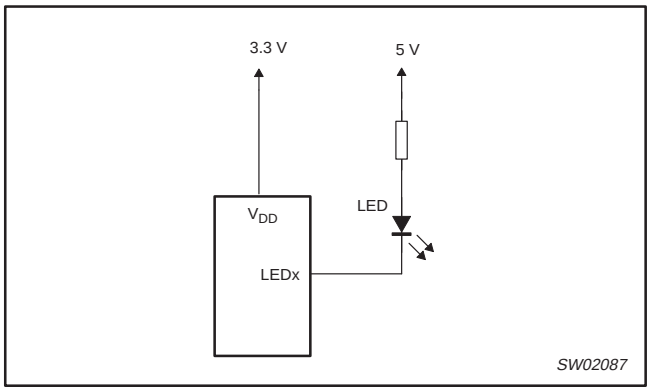


Figure 13. Device supplied by a lower voltage

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	6.0	V
$V_{I/O}$	DC input current on an I/O		V_{SS} – 0.5	6	V
$I_{I/O}$	DC output current on an I/O		—	± 50	mA
I_I	DC input current		—	± 20	mA
I_{DD}	Supply current		—	160	mA
I_{SS}	Supply current		—	200	mA
P_{tot}	Total power dissipation		—	200	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz; I/O = inputs	—	135	200	μA
I_{stbl}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	μA
I_{stbh}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	μA
V_{POR}	Power-on reset voltage (Note 1)	No load; $V_I = V_{DD}$ or V_{SS}	—	1.5	1.65	V
input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		–0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	+1	μA
C_I	Input capacitance	$V_I = V_{SS}$	—	6	10	pF
I/Os						
V_{IL}	LOW-level input voltage		–0.5	—	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3–5.5 V; Note 2	8	8–20	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3–5.5 V; Note 2	10	10–24	—	mA
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA; V_{DD} = 2.3 V; Note 3	1.8	—	—	V
		I_{OH} = –10 mA; V_{DD} = 2.3 V; Note 3	1.7	—	—	V
		I_{OH} = –8 mA; V_{DD} = 3.0 V; Note 3	2.6	—	—	V
		I_{OH} = –10 mA; V_{DD} = 3.0 V; Note 3	2.5	—	—	V
		I_{OH} = –8 mA; V_{DD} = 4.75 V; Note 3	4.1	—	—	V
		I_{OH} = –10 mA; V_{DD} = 4.75 V; Note 3	4.0	—	—	V
I_{IH}	Input leakage current	V_{DD} = 5.5 V; $V_I = V_{DD}$	—	—	1	μA
I_{IL}	Input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$	—	—	–1	μA
C_I	Input capacitance		—	3.7	5	pF
C_O	Output capacitance		—	3.7	5	pF
Interrupt $\overline{INT}$						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
Select Inputs A0, A1, A2						
V_{IL}	LOW-level input voltage		–0.5	—	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	—	5.5	V
I_{LI}	Input leakage current		–1	—	1	μA

NOTES:

1. V_{DD} must be lowered to 0.2 V in order to reset part.
2. Each I/O must be externally limited to a maximum of 25 mA and each octal (I/O0.0 to I/O0.7 and I/O1.0 to I/O1.7) must be limited to a maximum current of 100 mA for a device total of 200 mA.
3. The total current sourced by all I/Os must be limited to 160 mA.

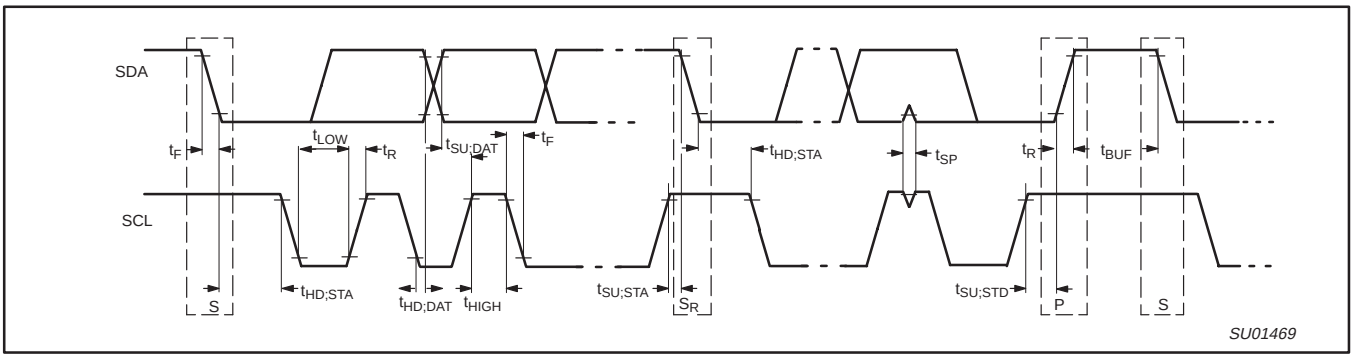


Figure 14. Definition of timing

AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	µs
$t_{VD;ACK}$	Valid time of ACK condition[2]	0.3	3.45	0.1	0.9	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;DAT}$	Data out valid time[3]	300	—	50	—	ns
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	$20 + 0.1C_b$ [1]	300	ns
t_R	Clock/Data rise time	—	1000	$20 + 0.1C_b$ [1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data set-up time	150	—	150	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Interrupt Timing						
t_{IV}	Interrupt valid	—	4	—	4	µs
t_{IR}	Interrupt reset	—	4	—	4	µs

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
4. t_{PV} measured from $0.7V_{DD}$ on SCL to 50% I/O output.

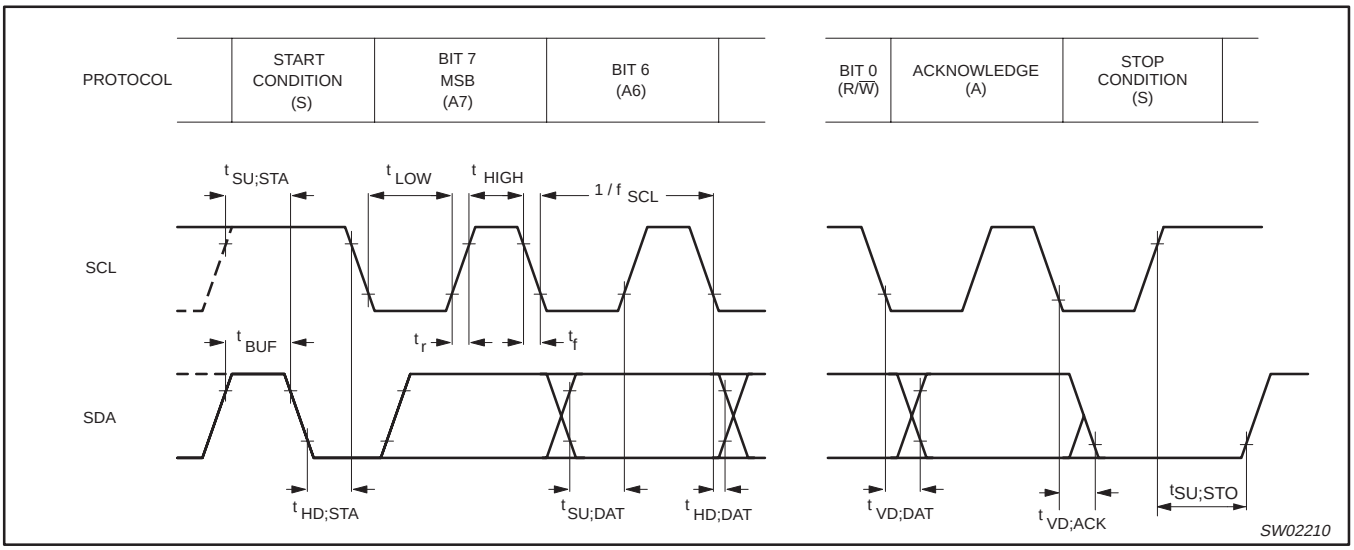


Figure 15. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

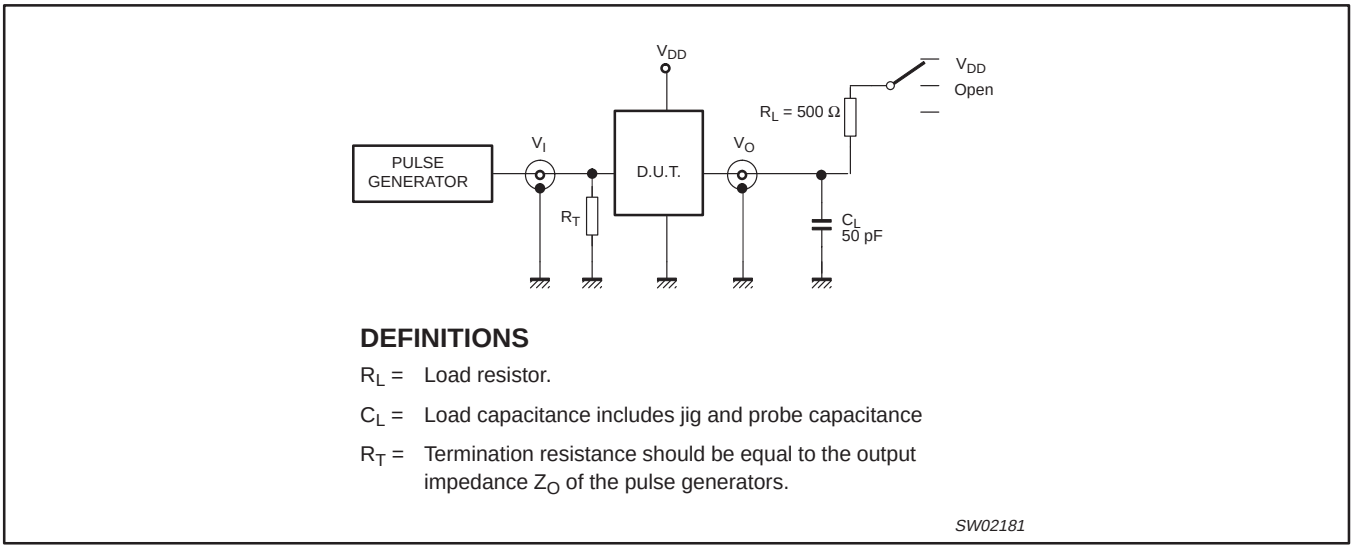
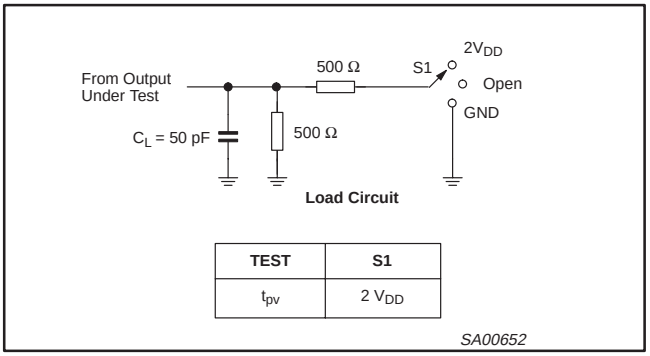


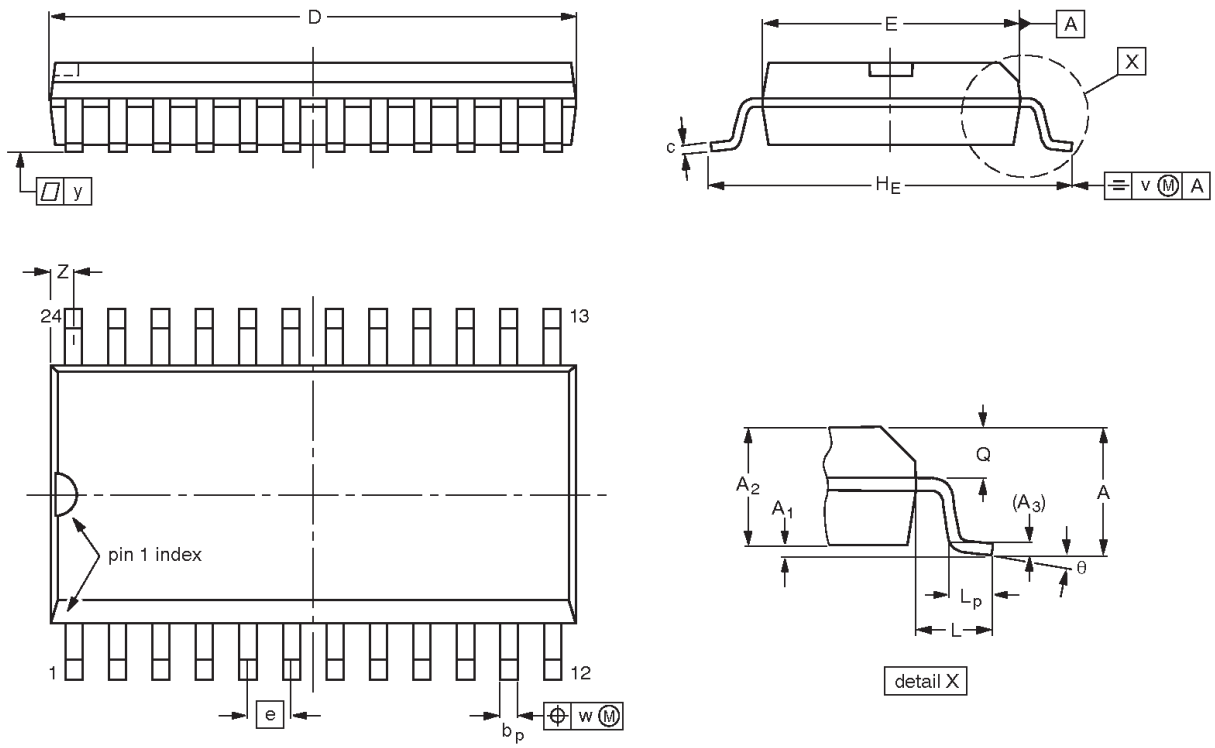
Figure 16. Test circuitry for switching times



TEST	S1
t_{pv}	2 V_{DD}

Figure 17. t_{PV} set-up conditions

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

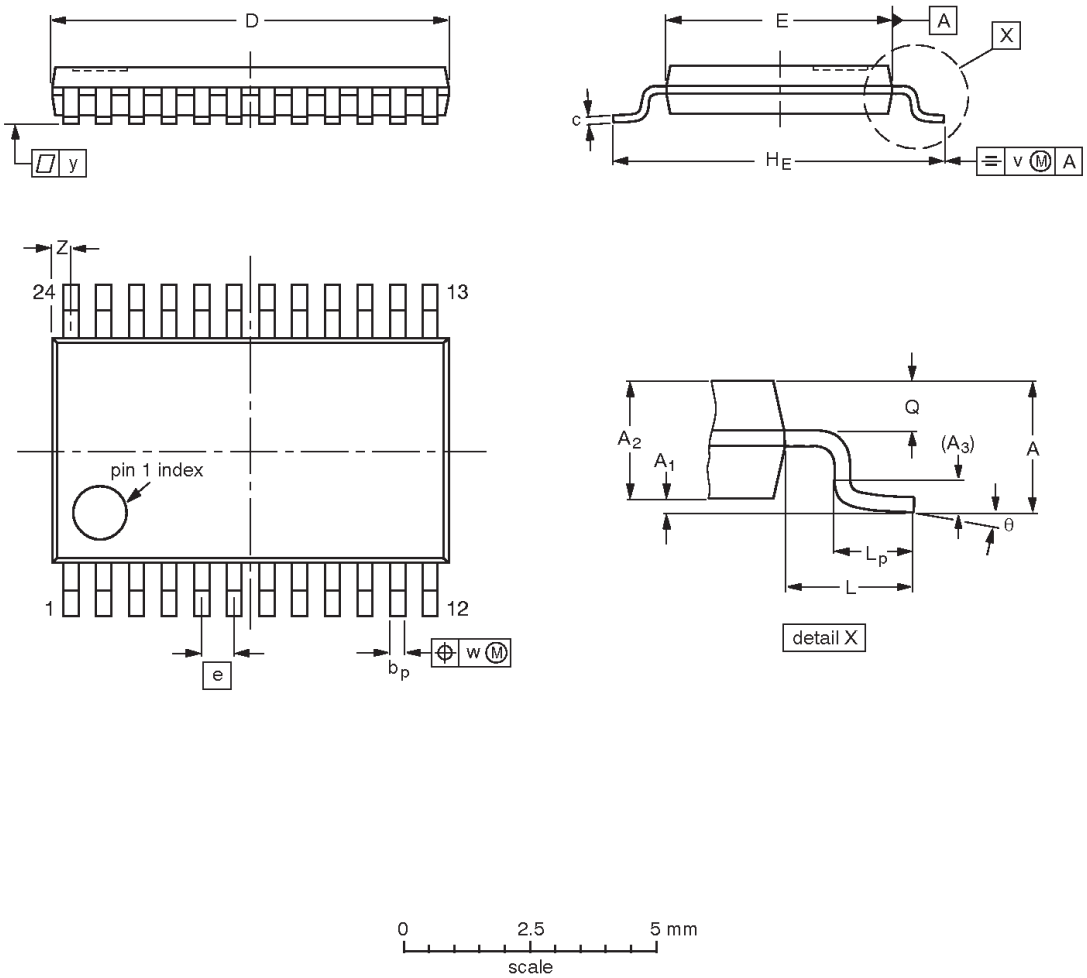
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1



DIMENSIONS (mm are the original dimensions)

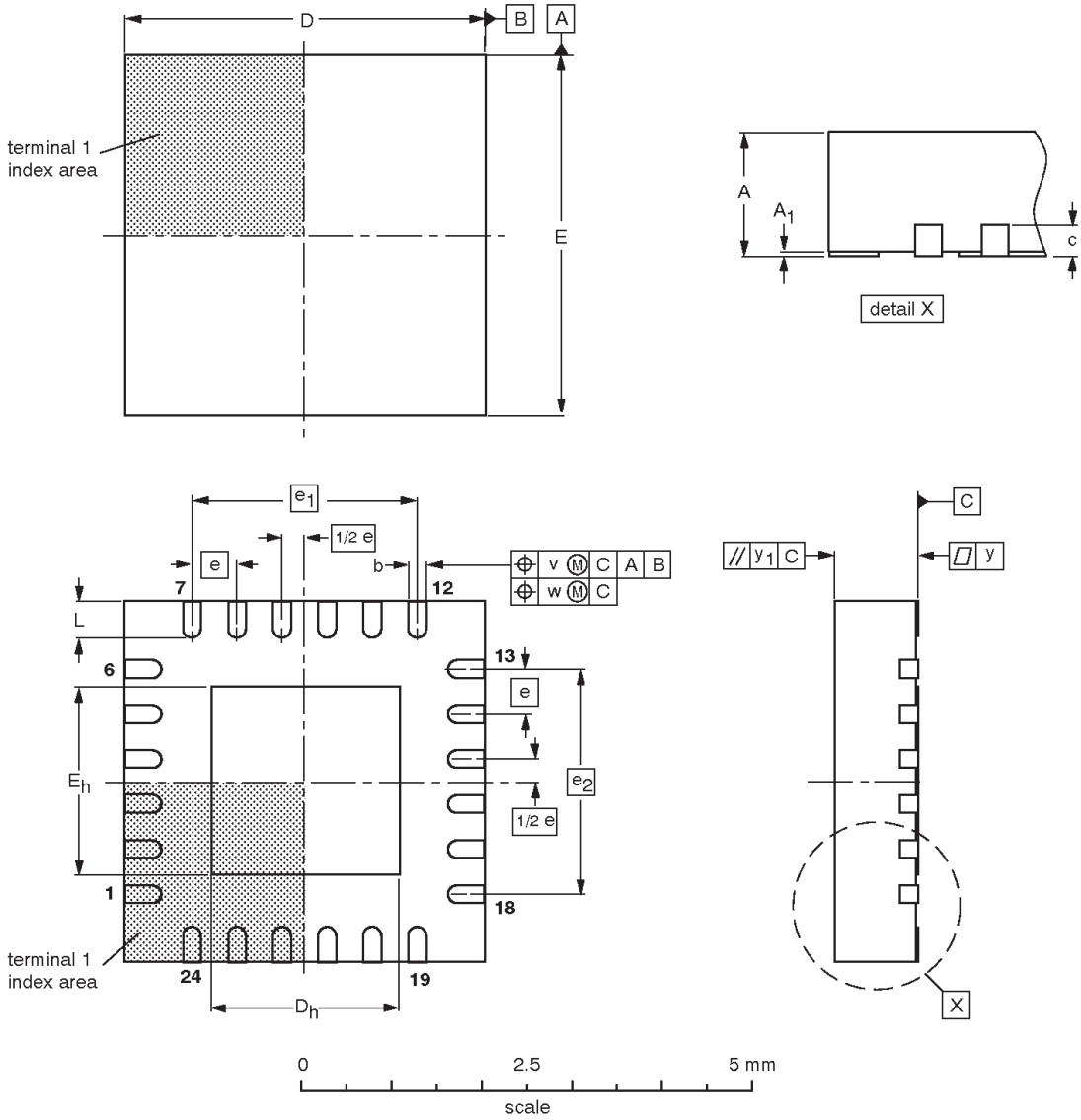
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_2	20040930	**Product data (9397 750 12896); Supersedes data of 2003 Jun 27 (9397 750 11681).** Modifications: ● Section “Registers 0 and 1—Input Port Registers” on page 6: add register bit table and second paragraph. ● “Power-on Reset” section on page 6 re-written. ● Figure 11 modified. ● “DC Characteristics” table on page 13: – sub-section “I/Os”: change V_{IL} (max) from 0.8 V to $0.3V_{DD}$ change V_{IH} (min) from 2.0 V to $0.7V_{DD}$ – sub-section “Select inputs A0, A1, A2: change V_{IL} (max) from 0.8 V to $0.3V_{DD}$ change V_{IH} (min) from 2.0 V to $0.7V_{DD}$ – Add (new) Note 1 – Note 2 re-written.
_1	20030627	**Product data (9397 750 11681); ECN 853-2430 30019 dated 11 June 2003.**

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Level	Data sheet status [1]	Product status [2] [3]	Definitions
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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